Amendments to the Claims

This listing of claims will replace all prior versions and listings of claims in the application:

Listing of claims:

1. (canceled)

2. (previously presented) The method of claim 7 wherein the control bit is set by a programmer.

3. (previously presented) The method of claim 7 further comprising:

handling the output signal as an STS connection when the control bit is set.

4. (previously presented) The method of claim 7 further comprising:

assembling the output signal from multiple VT/TU connections when the control bit is not set.

5. (previously presented) The method of claim 7 further comprising:

handling the output signal as the AU connection when the control bit is not set.

6. (previously presented) The method of claim 7 further comprising:

assembling the output signal from multiple VT connections when the control bit is set.

7. (Currently Amended) A method of processing an output signal comprising:

checking a state of a control bit that specifies whether to assemble the output signal from multiple virtual tributary connections or handle the output signal as an synchronous transport signal (STS) or administrative unit (AU) connection;

switching a predetermined number of connection entries together based on the state of the control bit;

storing the control bit in a connection memory;

checking a state of a second control bit that is associated with independent and concatenated payloads; and

~~checking the second control bit only~~ cross-connecting a second payload with a first payload if the second control bit is set.

8. (previously presented) The method of claim 7 further comprising storing the control bit in a register.

9. (canceled)

10. (canceled)

11. (canceled)

12. (Currently Amended) The method of claim 7 further comprising:

~~cross-connecting~~ processing a second payload ~~with~~ independently of a first payload if the second control bit is not set.

13. (previously presented) The method of claim 7 further comprising storing the second control bit in a connection memory.

14. (previously presented) The method of claim 7 further comprising storing the second control bit in a register.

15. (canceled)

16. (canceled)

17. (previously presented) The core logic of claim 18 wherein the control bit is set by a programmer.

18. (Currently Amended) A core logic and memory for provisioning cross-connects in an output signal in network switching environment comprising instructions for causing a computer said core logic to:

check a state of a control bit that specifies whether to assemble the output signal from multiple virtual tributary/tributary unit (VT/TU) connections or handle the output signal as an synchronous transport signal (8T8) or administrative unit (AU) connection;

switch a predetermined number of connection entries together based on the state of the control bit;

store the control bit in a connection memory;

check a state of a second control bit that is associated with independent and concatenated payloads; and

~~check the second control bit only~~ cross-connecting a second payload with a first payload if the second control bit is set.

19. (previously presented) The core logic of claim 18 further comprising instructions to store the control bit in a register.

20. (canceled)

21. (Currently Amended) The core logic of claim ~~20~~18 further comprising instructions to store the second control bit in a connection memory.

22. (Currently Amended) The core logic of claim ~~20~~18 further comprising instructions to store the second control bit in a register.

23. (canceled)

24. (Currently Amended) Apparatus for processing an output signal comprising:

a first memory storing a control bit that specifies whether to assemble the output signal from multiple virtual tributary (VT) connections or handle the output signal as an synchronous transport signal (8T8) or administrative unit (AU) connection;

a circuit to check a state of the control bit; and

control circuitry that uses a second memory to switch a predetermined number of connection entries together based on the state of the control bit;

a memory storing a second control bit that is associated with independent and concatenated payloads; and

a circuit to ~~check a state of the second control bit only~~ cross-connect a second payload with a first payload if the control bit is set.

25. (previously presented) The apparatus of claim 24 wherein the control circuitry is configured to handle the output signal as an STS connection when the control bit is set.

26. (previously presented) The apparatus of claim 25 wherein the control circuitry is configured to assemble the output signal from multiple VT connections when the control bit is not set.

27. (Currently Amended) The apparatus of claim 24 wherein ~~the first memory stores a second control bit that specifies whether payloads are independent or concatenated, and~~ the control circuit is configured to switch a predetermined number of payloads together based on the state of the second control bit.